

REMARKS

Claims 1-20 are pending in this application. Claims 1, 9, 14-17 and 19-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al (hereinafter Miller) (US Patent 4,368, 434). Claims 2-3 and 10-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in further view of Applicant's Admitted Prior Art (hereinafter Prior Art). Claims 4-8 and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in further view of Warren et al. (hereinafter Warren) (U.S. patent 6,075,807). Claims 1, 14 -15 stand rejected 35 U.S.C. 103(a) as being unpatentable over Warren. Claims 1, 14 -15 stand rejected 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Alexander (US patent 6,765,419 B2).

Without limitation of the claims, the disclosed embodiments pertain to digital processing of data samples and to data path latency due to processing of samples through delay chains. Delay chains are introduced within digital systems to allow for various transient processing operations, such as timing recovery of samples' boundaries in the case of data packets. However, the processing of samples through such delay chains, subsequent to the transient processing events that required them, may unnecessarily add to the data path latency and, consequently, lead to suboptimal performance. Disclosed embodiments provide for reduction of the data path latency via reduction of the length of such delay chains once the transient processing operations are completed. In particular, dynamic reduction of the length of a delay chain no longer required is provided by eliminating delay elements from the delay chain, which is achieved by first shifting samples out of the delay chain at an output rate higher than an input rate of reading additional samples into the delay chain.

Rejection of Claims 1, 9, 14 -17 and 19-20 Under 35 U.S.C. § 103(a) as unpatentable over Miller

The Examiner has rejected claims 1, 9, 14 -17 and 19-20 under 35 U.S.C. 103(a) as being unpatentable over Miller.

With respect to previous claim 1, the Examiner indicates that Miller fails to explicitly disclose the limitations of “in response to receiving a signal of completion of a processing event, shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain”, and “dynamically reducing the length of the clocked delay chain as data samples continue to be read into the clocked delay chain”. Nonetheless, despite Applicant’s previous arguments, the Examiner indicates that it would have been obvious to one of ordinary skills in the art to incorporate Miller features such as mode control, CLOCK SELECT and DELAY SELECT signals into the system of Miller, in the manner as claimed.

In particular, the Examiner appears to regard a change in communication protocol as a processing event, as claimed in previous claim 1. For clarity, Applicant has amended claim 1 to recite “a transient processing operation on data samples”, instead of “a processing event”. in order to draw a clearer distinction from the Miller disclosure. Applicant contends that the mode select or change in communication protocol of Miller is not a ‘transient processing operation on data samples’.

Further, the Applicant has amended claim 1 to be directed at a “method of reducing data path latency in digitally processing a sequence of data samples, the data path latency being associated with a transient processing operation on the data samples” in order to further distinguish from Miller.

Also, Applicant maintains that Miller, in particular the mode control, does not suggest “shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain”. The Examiner indicated that an increase of the rate of the Miller delay line would mean that the output rate is greater than the input rate. Applicant disagrees. The Miller delay line has a single rate, throughout its length, and therefore the same rate at output and input. Miller does teach adjusting the rate, but this does not suggest in any way a different rate at output than at input, as claimed in claim 1.

Based on at least this reasoning, the Applicant believes that Claim 1 is patentable in view of the Miller reference. The Applicant further contends that independent apparatus claim 14

corresponding to method claim 1 is patentably distinct over Miller et al. for at least the same reasons.

Even further, Applicant contends that apparatus claim 9 and method claim 15, which recite limitations of claim 1, in the same or similar language, are also patentably distinct over Miller et al. for reasons presented in regards to claim 1.

As claims 16-17 and 19-20 are dependent on claims 14 and 15 and incorporate their limitations, the Applicant respectfully asserts that these claims are also allowable over Miller et al., in light of the arguments above.

Rejection of Claims 2-3 and 10-11 Under 35 U.S.C. § 103

Claims 2-3 and 10-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in further view of Applicant's Admitted Prior Art (hereinafter Prior Art). Claims 4-8 and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. in further view of Warren et al. (hereinafter Warren) (U.S. patent 6,075,807). The Applicant respectfully traverses this rejection for the following reasons.

The Applicant incorporates the arguments above distinguishing amended claim 1 from Miller et al. Furthermore, Applicant contends that neither of the remaining cited references, Applicant's Prior Art and Warren et al., teach or otherwise suggest the limitations of amended claim 1.

As claims 2-8, 10-11 and 13 are dependent on claim 1 and incorporate its limitations, the Applicant respectfully asserts that Miller, Applicant's Prior Art and Warren et al., taken alone or in combination, fail to teach, suggest or otherwise render obvious claims 2-8, 10-11 and 13. Therefore, Applicant asserts that claims 2-8, 10-11 and 13 are also allowable over the cited art.

Rejection of Claims 1, 14-15 under 35 U.S.C. § 103(a) as unpatentable over Warren

The Examiner has rejected claims 1, 14 and 15 under 35 U.S.C. 103(a) as being unpatentable over Warren.

Regarding previous claim 1, the Examiner notes that Warren fails to explicitly teach “in response to receiving a signal of completion of a processing event, shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain”, and “dynamically reducing the length of the clocked delay chain as data samples continue to be read into the clocked delay chain” but contends that Warren suggests these limitations as it discloses adjustment of the propagation rate of the delay line after synchronization has been achieved.

Applicant respectfully notes that *an adjustment of the rate of a delay line* does not suggest in any way a reduction in the length of the line, nor different input and output rates, as claimed in previous and currently amended claim 1. Warren does not disclose nor otherwise suggest reducing the length of the delay line, nor a delay line with an input rate smaller than an output rate. As previously discussed, the difference in rates results in a gap in data within the delay line that can be used to drop delay elements to reduce the length of the delay chain.

Based on at least this reasoning, the Applicant believes that Claim 1 is patentable in view of the Warren reference. The Applicant further contends that independent apparatus claim 14 and method claim 15 are patentably distinct over Miller et al. for at least the same reasons.

Rejection of Claims 1, 14 -15 under 35 U.S.C. § 103(a) as unpatentable over Prior Art and Alexander

The Examiner has rejected claims 1, 14 and 15 under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Alexander.

Applicant has previously argued that Alexander is from a non-analogous art and therefore cannot be relied upon as a basis for rejection of the claimed invention. The Examiner has replied in the Office Action of February 28, 2008, indicating that Alexander can be relied upon since both applicant's and Alexander's disclosure deal with synchronization.

Applicant respectfully disagrees with this argument, as applicant's claimed invention deals not with synchronization, like Alexander, but with optimizing data path latency. In Alexander, an analog delay chain is adjusted for achieving synchronization between two clocks.

In Applicant's claimed invention, a clocked delay chain is reduced for reducing data path latency. The particular problem with which the Applicant is concerned is not achieving synchronization, as in Alexander; therefore, Oetoker, 977 F. 2d 1443 24 USPQ2d 1443 (Fed. Cir. 1992), previously cited by the Examiner, does not apply.

Accordingly, Applicant maintains that Alexander is from a different art than the Prior Art and these references cannot be combined in rejecting claims 1, 14 and 15. Nonetheless, even if Alexander and the prior art were combined, Applicant believes the combination does not teach, suggest, or make obvious the invention of amended Claim 1 as discussed below.

FIG. 1 in Alexander discloses a delay lock loop (DLL) circuit 10 that is used to align clock edges. The delay circuit does not receive a sequence of data samples, and there is no processing of data samples from taps on the delay. The circuit 10 compares a reference clock signal 22 to a feedback clock signal 24 and generates an output clock signal 26 by delaying the reference clock signal 22 via a forward delay circuit 12. The comparison and delay are iterated until the feedback clock 24 is aligned in time with the reference clock signal 22. (See column 3, lines 33-40.) A control signal 28 is used to increase, decrease or leave unchanged the amount of time by which the output clock signal 26 is delayed relative to the reference clock signal 22. (See column 4, lines 2024, and column 6, lines 8-18.) Therefore, the delay amount is adjusted, either by increasing it, decreasing it or leaving it unchanged, until the input and output clock edges match. In other words, in **Alexander, adjustment of the delay chain occurs while synchronization is incomplete**, and the adjustment is directed at achieving synchronization. In Alexander, **the delay chain is not adjusted in response to a signal of completion of a transient processing operation** on the data samples, as recited in amended claim 1.

Alexander does not teach nor otherwise suggest "in response to receiving a signal of completion of the transient processing operation on the data samples, shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain" as recited in amended Claim 1. Furthermore, this claim limitation is not taught nor otherwise suggested by the Prior Art

According, Applicants respectfully submit that Claim 1 is patentable over the Prior Art in view of Alexander. The Applicant further contends that independent apparatus claim 14 and method claim 15 are patentable over the Prior Art and Alexander for at least the same reasons.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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